EC	E3710 Exam 2. Name			
res	ring 2013. 5 pages. 102 points, but scored out of 100. You may use any non-living ource to complete this exam. Any hint of cheating will result in a 0.  t 1 – Short Answer			
1.	(2 pts) An original 8051 uses a 5.5296 MHz crystal. How long (in µs) is a machine cycle?			
2.	(2 pts) If an external clock is used, which pin of the 8051 should it be connected to?			
3.	(3 pts) The following line appears in an Intel HEX file: :020304001516CC (a) is the checksum valid?			
	(b) what address(es) will be affected?			
	(c) how many bytes of data does this line provide?			
4.	(2 pts) Write one line (in C or assembly) that configures timer 0 as a 16-bit <u>counter</u> and timer 1 as an 8-bit auto-reload timer (e.g. for baud rate generation).			
5.	(2 pts) If an 8051 has a 22.1184MHz crystal, and timer 1 has been configured in mode 2, what value should be loaded to TH1 to obtain a 12.8kHz overflow frequency?			
6.	(2 pts) If TMOD is set to 09H, what two conditions are required for timer 0 to run?  (a)			
	(b)			
7.	(1 pt) (true/false) Timer 2 (8052) can be configured as a 16-bit auto-reload timer.			
8.	<ul><li>(2 pts) The 8051 supports a 9-bit serial format. Why? (circle all that apply)</li><li>(a) to support the "8-bit data with parity, one stop bit" format.</li><li>(b) to support the "8-bit data, no parity, two stop bits" format</li><li>(c) to support the "7-bit data with parity, two stop bits" format."</li><li>(d) to enable a multi-processor communication feature.</li></ul>			
9.	(2 pts) Write one line (in C or assembly) that configures the serial port for 8-bit data, 1-bit parity and one stop bit.			
10.	(3 pts) Can an 8051 with a 5.5296 MHz crystal send and receive serial data at 9600 baud? If so, list the relevant SFRs and what they must be written to. If not, explain why not.			

	2. Assume the start bit begins at	
(a)		
		-ıııı-
6v - (b)		
	<sub> </sub> <sub> </sub> <sub> </sub>	-     -
-	) Name the 5 interrupt sources of include reset)	n the original 8051 and their interrupt vectors
,	upt:	Vector =
	upt:	
13. (1 pt) routin 14. (3 pts)	(true/false) If bit IT1 = 1, then II e) for external interrupt 1 return	E1 is cleared when the ISR (interrupt service s.  TF0 and TF1 when their associated ISRs are
13. (1 pt) routin 14. (3 pts) called  15. (2 pts)	(true/false) If bit IT1 = 1, then II e) for external interrupt 1 returns ) The 8051 automatically clears in the why doesn't it clear TF2 in the	E1 is cleared when the ISR (interrupt service s.  TF0 and TF1 when their associated ISRs are e same way?  ly) that configures the timer 2 interrupt, the
13. (1 pt) routin 14. (3 pts) called  15. (2 pts) serial  16. (2 pts) pendin priorit	(true/false) If bit IT1 = 1, then Ite) for external interrupt 1 returns ) The 8051 automatically clears in the work with the control of the second of the control of the co	E1 is cleared when the ISR (interrupt service s.  TF0 and TF1 when their associated ISRs are e same way?  ly) that configures the timer 2 interrupt, the to be high priority.  nal interrupt 1 are both low priority and become t is being serviced. Assuming no other high interrupt (timer 0 or external interrupt 1) will be
13. (1 pt) routin 14. (3 pts) called  15. (2 pts) serial  16. (2 pts) pendin priorit servic  17. (3 pts)	(true/false) If bit IT1 = 1, then Ite) for external interrupt 1 returns () The 8051 automatically clears in the work why doesn't it clear TF2 in the interrupt and external interrupt () () Write one line (in C or assembly interrupt and external interrupt () () Suppose that timer 0 and external while a high priority interrupt interrupts are pending, which ed when the high priority interrupts	E1 is cleared when the ISR (interrupt service s.  TF0 and TF1 when their associated ISRs are e same way?  By) that configures the timer 2 interrupt, the to be high priority.  In all interrupt 1 are both low priority and become t is being serviced. Assuming no other high interrupt (timer 0 or external interrupt 1) will be upt returns?  In all interrupt service routine returns using the RET

20.	(4 pts) When <u>data</u> are written to an LCD controller, what is the state of the following four signals? (Answer H or L.)
21.	$CS = $ $RD = $ $WR = $ $RS (A_0) = $ (2 pts) Name 3 different types of A/D converter we discussed in class:
22	(4 pts) A 14-bit A/D converter uses a 1.5v positive reference and a 0.1v negative
22.	reference.  (a) What is its step size?  (b) What is the output of the A/D if its input is 0.85v?
23.	(3 pts) A certain 12-bit A/D converter uses sample and hold circuit and an analog multiplexer to select one of several input channels. The sampling capacitance is 20pF and the resistance through the MUX is $3.4k\Omega$ . If the desired sample accuracy is ½ of an LSB and the source resistance is $12.5k\Omega$ , how long must the input channel be selected before the conversion can begin?
24.	(2 pts) Which of the following quantities are commonly used to characterize a <u>DAC</u> (circle all that apply): (a) resolution (b) conversion time (c) step size (d) capacity
25.	(4 pts) An 8-bit DAC has $V_{ref}^+$ = 10.0V and $V_{ref}^-$ = 0V.
	(a) What is its step size?
	(b) What voltage will it output if its input is 70H?

## Part 2 - Problems

26. (5 pts) Fill in the missing entries for the semiconductor memories shown below:

Type	Organization	Capacity	Address Pins	Data Pins
SRAM		256K	16	
DRAM	4M x 1			
EPROM		512K		8
	256Kx8		10	

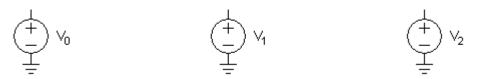
27. (6 pts) A certain type of oxygen sensor generates 13 mV per percent O<sub>2</sub>. The offset voltage (the output of the sensor at 0% O<sub>2</sub>) is 0.15V. If the A/D converter in problem 22 is used with this sensor, find an equation to convert the output of the A/D to oxygen level (in percent) using the form:

$$PO_2 = \frac{m(AtoD - k)}{2^{16}}$$

Find k and m (round to the nearest integer).

_		
k =	1/1 —	
Λ —	m =	

28. (3 pts) Draw an R/2R Resistor network for a 3-bit DAC.



29. (4 pts) Write an interrupt service routine in assembly for timer 0 that toggles P2.0 once every 72 interrupts.

org 0BH
jmp timer0\_int ; timer 0 interrupt

timer0\_int:

30. (12 pts) A Caesar (or shift) cipher encodes a character by shifting its position in the alphabet by a fixed amount. For example, if the shift is 3, A→D, B→E, ... W→Z, X→A, Y→B and Z→C. Write a program to run on the C8051F020 that receives characters over the serial port, performs a Caesar cipher (shift 3) on the upper-case alphabetic characters (A-Z), and sends the encrypted characters back through the serial port. (All other characters are echoed without encryption.) Your code may assume the 22.1184MHz crystal is running, but it must initialize the timer(s), serial port and interrupts. Once the configuration is complete, all work must be done inside the interrupt service routine(s). You may write this code in assembly or C. It is recommended that since this is a take-home exam, you should test your code in Lab 418, print off a copy and staple it to this exam. Otherwise, if you are feeling lucky, write your code on the back of this page and call it good.

31. (12 pts) You are designing a system using the C8051F020 to replace an obsolete system that uses an old 8051. In order to minimize the impact in software, you must use the same memory map as the original system, which is shown below. You will use a 32Kx8 Static RAM, an 8Kx8 ROM, and a 256x8 NVRAM with RD, WR and CS all active low. The LCD module is the same as the one we used in our class project. Show a schematic of the system including the external bus (address, data and control), address decoder, memories, LCD module, decoding circuitry and address latch, if necessary. Make sure to label the ports on the C8051F020. Draw busses with a single line and name their bits (e.g. A<sub>7</sub>-A<sub>0</sub>). Finally, State the value that must be stored in EMI0CF for your schematic to work. (Note: it is OK if something happens to be mapped into the "Not Used" regions since the old software never accesses those locations anyway.)

0000	Static
7FFF	RAM
8000	NV
807F	RAM
8080	Not
9FFF	Used
A000	LCD
A001	Module
A002	Not
DFFF	Used
E000	ROM
FFFF	